Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 2, 4, 5, 11, 15, 16, 19, 21, 23, 24, 26 and 27 have been amended. Claims 3 and 12-14 have been cancelled. Therefore, claims 1, 2, 4-11 and 25-28 are presented for examination.

The drawings stand objected under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claim 1, line 4, "an execution unit coupled to the instruction buffer and the first MO buffer" must be shown or the feature(s) canceled from the claim(s). In addition, the drawings stand objected to because in Figure 3, "INSTRUCTION DECODE" should read --INSTRUCTION DECODE MODULE--; and "INSTRUCTION EXECUTION" should read --INSTRUCTION EXECUTION UNIT-- in order to be consistent with the description of the specification. A replacement Figure 3 has been submitted herewith.

Claims 16-18, 23 and 28 stand objected to because of various informalities. Applicant submits that claims 16, 23 and 28 have been amended to be appear in proper condition for allowance.

Applicant acknowledges that claims 4-10, 14-18, 22, 23, 27 and 28 would be allowable if rewritten to overcome the various rejections and objections.

Claims 19-23 and 26-28 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant submits that claims 19 and 28 have been amended to appear in proper condition for allowance.

Claims 1-3, 19-21 and 24-26 stand rejected under 35 U.S.C. §102(b) as being anticipated by Shiell et al. (U.S. Patent No. 5,935,241). Applicant submits that the present claims are patentable over Shiell.

Shiell discloses a data processing system having a microprocessor. The microprocessor includes three levels of internal cache memory, a microcache, a look-aside buffer (TLB) that controls memory accesses to the cache and a main memory. A decoder within the microprocessor is also disclosed. See Shiell at Figure 1.

Claim 1 of the present application recites a decode module to decode an instruction to determine whether the instruction is to be stored in a first MO buffer. Applicant submits that nowhere in Shiell is there disclosed that the decoded decodes an instruction to determine whether the instruction is to be stored in a buffer. Therefore, claim 1 is patentable over Shiell.

Claims 2 and 4-10 depend from claim 1 and include additional features. Thus, claims 2 and 4-10 are also patentable over Shiell.

Claim 11 recites a decode module to decode an instruction to determine whether the instruction is to be stored in the first MO buffer or the second MO buffer. Thus, for the reasons described above with respect to claim 1, claim 11 is also patentable over Shiell. Since claims 15-18 depend from claim 11 and include additional features, claims 15-18 are also patentable over Shiell.

Claim 19 recites examining a bit within a first instruction to determine whether the first instruction is to be retrieved from a first buffer. Applicant submits that nowhere in Shiell is there disclosed a process of examining a bit within an instruction to determine if the instruction is to be stored within a buffer. As a result, claim 19 is patentable over Shiell. Because claims 20-23 depend from claim 19 and include additional features, claims 20-23 are also patentable over Shiell.

Claim 24 recites a program of instructions when executed by a processing unit causes the processing unit to examine a bit within a first instruction to determine whether the first instruction is to be retrieved from a first buffer. Therefore, for the reasons described above with respect to claim 19, claim 24 is also patentable over Shiell. Since claims 25-28 depend from claim 24 and include additional features, claims 25-28 are also patentable over Shiell.

Claims 11-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shiell et al. in view of Pechanek et al. (U.S. Patent No. 5,682,491). Applicant submits that the present claims are patentable over Shiell even in view of Pechanek.

Pechanek discloses an array processor topology reconfiguration system that enables processor elements in an array to dynamically reconfigure their mutual interconnection for the exchange of arithmetic results between the processors. See Pechanek at Abstract. Nonetheless, Pechanek does not disclose or suggest a decode module to decode an instruction to determine whether the instruction is to be stored in a first MO buffer. Moreover, Pechanek does not disclose or suggest examining a bit within a first instruction to determine whether the first instruction is to be retrieved from a first buffer.

As discussed above, Shiell does not disclose or suggest such features. Therefore any combination of Shiell and Pechanek would not disclose or suggest a decode module to decode an instruction to determine whether the instruction is to be stored in a first MO buffer, or examining a bit within a first instruction to determine whether the first instruction is to be retrieved from a first buffer. Therefore, the present claims are patentable over Shiell in view of Pechanek.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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